



UNIVERSITÉ  
LAVAL

## All Silicon IQ Modulator with 1Tb/s Line Rate

Sasan Zhalehpour, Mengqi Guo, Jiachuan Lin, Zhuhong Zhang, Hassan Sepehrian, Yaojun Qiao, Wei Shi, and Leslie A. Rusch

IEEE/OSA Optical Fiber Communications Conference (OFC 2020)

© 2020 IEEE/OSA. Personal use of this material is permitted. Permission from IEEE/OSA must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

# All Silicon IQ Modulator with 1Tb/s Line Rate

Sasan Zhalehpour<sup>1</sup>, Mengqi Guo<sup>2</sup>, Jiachuan Lin<sup>3</sup>, Zhuhong Zhang<sup>3</sup>,  
Hassan Sepehrrian<sup>3</sup>, Yaojun Qiao<sup>2</sup>, Wei Shi<sup>1</sup>, and Leslie A. Rusch<sup>1\*</sup>

<sup>1</sup>ECE, COPL, Université Laval, Canada, <sup>2</sup>Beijing University of Posts and Telecomm., China,

<sup>3</sup>Huawei Technologies Canada Co., Ltd., ON, Canada

\*rusch@gel.ulaval.ca

**Abstract:** By significantly improving the accuracy of our nonlinear pre-compensation digital signal processing, we achieve 1 Tb/s line rate with an all silicon modulator using 32QAM modulation with dual polarization emulation. © 2019 The Author(s)

**OCIS codes:** 060.4510, 060.1660, 060.2360.

## 1. Introduction

Next generation cloud infrastructures and data centers require higher optical communications capacity to enable bandwidth-hungry services. Operating optical coherent systems at 100 Gbaud and beyond with integrated optical MZMs has been demonstrated for lithium niobate (LiNbO<sub>3</sub>) [1], indium phosphide (InP) [2], and silicon photonics (SiP) [3]. Despite compatibility with complementary metal-oxide semiconductor (CMOS), SiP comes with challenges of nonlinear frequency response, higher insertion loss, and lower modulation efficiency and bandwidth.

SiP requires system optimization to attain high-quality quadrature amplitude modulation (QAM) using a depletion-mode silicon modulator [4]. Recently, the authors reported a depletion mode all-silicon single-carrier 16QAM and 32QAM modulation at 100 Gbaud on a single polarization [3]. In this work, we have significantly improved the accuracy of our nonlinear predistortion (the mean square error in adaptation is reduced by an order of magnitude) vis-à-vis previous results. This allows us to obtain equal, if not better, BER results at dual polarization compared to those at single polarization. Using polarization emulation, we achieved a 1 Tb/s line rate, 32QAM modulation with an all silicon modulator. Our bit error rate (BER) is below the 20% forward error correction (FEC) threshold. To the best of our knowledge, this is the first demonstration of 1 Tb/s line rate in a SiP modulator.

## 2. Modulator operation (linear compensation)

Distortion caused by bandwidth limited components, *e.g.*, MZM and digital-to-analog converter (DAC), is first addressed with linear compensation. As part of the linear compensation, we find the optimal operating voltage of the modulator and optimally split the linear compensation at the transmitter across both digital and optical filters.

Our depletion-mode SiP IQ modulator has two nested MZMs with traveling-wave electrodes applied. The small-signal response ( $S_{21}$ ) shows a strong dependence on the DC bias. The 3-dB bandwidth is  $\sim 22$  GHz at zero bias,  $\sim 26$  GHz at  $-0.75$  V, and  $\sim 34$  GHz at  $-4$  V. Furthermore, the modulation efficiency decreases as the bandwidth increases. Design details can be found in [4, 5].

The intersymbol interference (ISI) encountered at 100 Gbaud is compensated by both digital and optical filters. First, we linearize the frequency response of the DAC by a digital minimum mean square error (MMSE) filter. Next, a programmable optical bandpass filter (OBF) is used to linearly compensate the roll-off of the frequency response of the MZM in the optical domain. We sweep the depth of the optical OBF to minimize bit error rate (BER) and fix that value for the rest of the experiment.

We sweep the DC bias voltage (always optimizing linear compensation at each point) to trade-off modulation efficiency and bandwidth, using BER as our figure of merit. The BER results are presented in Fig. ??b, where a clear minimum is visible at  $-2$  V.

## 3. Experimental set-up and signal processing

Figure 1 illustrates the experimental set-up and offline DSP processing. The central, lower DSP blocks represent quasi real-time adaptive predistortion described in section 4. The two outputs of a wideband DAC (Micram, DAC10004: 40 GHz, 6 bits, and 100 GSa/s), carrying the in-phase and quadrature components of an M-QAM signal, are de-skewed in time via tunable RF phase shifters (PS) before being amplified with 50 GHz, 18 dBm RF drivers. The outputs of RF drivers are fed to the modulator by a ground signal-signal ground (GS-SG) configured RF probe. The operating point is set at the null point by adjusting the DC voltage of thermo-optic phase shifters.

A tunable external cavity laser (ECL), with linewidth less than 100 kHz and wavelength 1530 nm, is coupled to the silicon chip via a fiber array. To overcome the coupling loss (9 dB) and modulator loss (6.8 dB), a high power

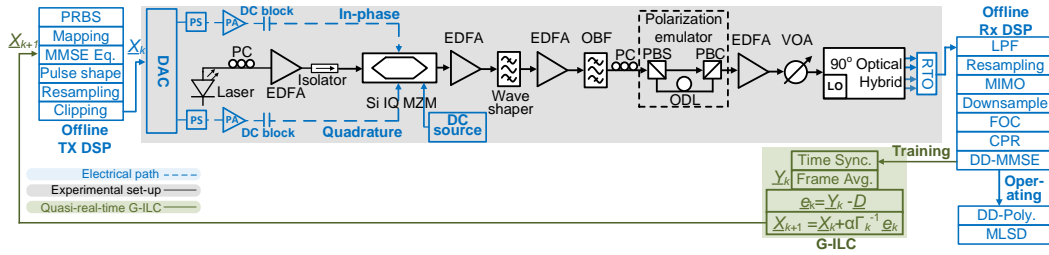


Fig. 1: Block diagram of the experimental set-up (grey shading) and offline DSP.

erbium doped fiber amplifier (EDFA) boosts the laser power from 10 dBm to 26 dBm. In addition, the optical output of the modulator is amplified by several EDFAs to combat loss.

The OBF optimized per the previous section is used for optical pre-emphasis. Another OBF suppresses out-of-band amplified spontaneous emission from EDFAs. A dual polarization emulator, consisting of a polarization beam splitter (PBS), a polarization beam combiner (PBC), and an optical delay link (ODL), is employed to demonstrate the dual polarization modulation. All experiments are back-to-back. A  $90^\circ$  hybrid, four photodetectors (70 GHz) and a local oscillator (LO; 16 dBm) form the receiver. The optical power is swept by a variable optical attenuator (VOA). The electrical outputs are digitized by a real-time oscilloscope (RTO) (160 GSa/s, 63 GHz).

A pseudo random bit sequence (PRBS) of length  $2^{19} - 1$  (PRBS19) is Gray mapped and passed through the minimum mean square error (MMSE) digital predistortion filter, upsampled and pulse shaped to a raised cosine filter with roll-off of 0.01. The signal is resampled to the sampling rate of the DAC before being clipped and quantized. At the receiver side, the signal is filtered by a  $10^{th}$  order super Gaussian digital low-pass filter (LPF) and the captured 1.6 samples per second are upsampled to 2 samples per symbol. We use  $4 \times 4$  multiple-input multiple-output (MIMO) for joint I/Q polarization demultiplexing; they are run at T/2 spacing to provide accurate timing, and then downsampled to one sample/symbol for all other processing. Frequency offset compensation (FOC) is performed blindly by a fast Fourier transform (FFT), carrier phase recovery (CPR) is a blind phase search with 64 test angles, and finally a decision-directed (DD) MMSE filter.

#### 4. Nonlinear compensation and Results

Nonlinear processing at both transmitter and receiver reduces residual nonlinearity (introduced by the SiP MZM, photodetectors, limited effective number of bits in the RTO and DAC, RF amplifier, etc.) after standard linear processing. The pre-distortion is found adaptively during the training phase of a gain-based iterative learning control (G-ILC) algorithm. The G-ILC, whose adaptation is described in the next section, is the most important processing step enabling 100 Gbaud modulation [3]. Combining the G-ILC at the transmitter with nonlinear post-compensation at the receiver side allows extra margin.

We concatenate blind nonlinear techniques: decision-directed memory polynomial followed by a paired low pass filter/maximum likelihood sequence detector (MLSD); see Fig. 1. The memory polynomial, a simplified Volterra series, uses only 1<sup>st</sup> and 3<sup>rd</sup> order terms [7]. Other Volterra solutions were attempted, but with modest improvement that did not justify added complexity. The second step introduces structured, known ISI via a one-tap noise whitening filter. That ISI is treated via the lowest order complexity (one symbol) MLSD [?]. Heuristically, the in-band noise enhancement is undone by the noise whitening filter, and the MLSD overcomes residual nonlinear effects ensnared in the structured ISI. The MLSD is implemented via the computationally efficient Viterbi algorithm. The combined memory polynomial and MLSD approach complement the workhorse G-ILC.

##### 4.1. G-ILC evaluation

Our first results pertain to the adaptation of the G-ILC pre-compensation. The achievement of 1 Tb/s modulation was only possible due to an order of magnitude reduction in the mean squared error of the pre-distorted signal. As detailed in [6], the G-ILC operates on a fixed data sequence that is transmitted repeatedly. At reception, additive white Gaussian noise is reduced via averaging over multiple copies of the sequence. Noise-averaged data is compared to the transmitted sequence, and a correction error vector is calculated. During the pseudo-real-time adaptation with hardware-in-the-loop, we find the optimal pre-distorted signal. By accessing a signal clear of linear distortion and additive noise, the G-ILC error signal can address the residual impairments more directly.

While the OSNR margin offered with data-aided (DA) MMSE for adaptation was sufficient for single-polarization [3], it did not meet the dual-polarization requirement for higher OSNR. We incorporated a data-aided (DA)  $2 \times 2$  MIMO in the adaptation chain, which led to the dramatic increase in G-ILC effectiveness. A block di-

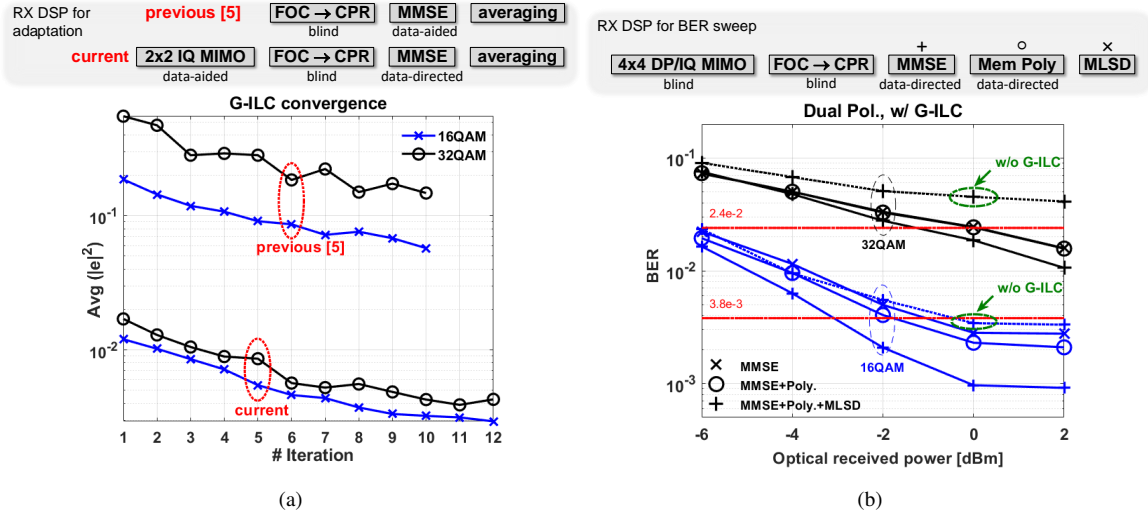


Fig. 2: (a) Convergence at 100 Gbaud for 16/32QAM; original [3] and improved, and (b) BER sweep for 100 Gbaud emulated DP-16/32QAM using G-ILC and post-compensation: DD-MMSE ( $\times$ ), adding memory polynomial ( $\circ$ ), adding MLSD (+); dotted line is best result w/o G-ILC.

agram of the two approaches is above the graph in Fig. 2a of convergence curves for G-ILC. Adaptation is always performed over a single polarization.

We see that the gap has closed between 16/32QAM error levels. The receiver offers a clear view of nonlinear impairments, even for closely packed 32-QAM symbols. More importantly, the order of magnitude reduction means the G-ILC is a much more effective pre-compensation. Adaptation slope is not adversely affected, and convergence occurs in 12 iterations.

#### 4.2. BER evaluation

Bit error rates (BER) are presented in Fig. 2b versus optical receiver power for 16QAM and 32QAM at 100 Gbaud. We provide BER for multiple scenarios to identify the relative importance of various combinations of our mitigation techniques. To establish the central importance of the G-ILC pre-compensation, we include in the dotted curves the scenario when no G-ILC is used. The dotted curve represents performance when all (TX and RX) linear and RX-side nonlinear techniques are used, but not the G-ILC; it under performs all cases where the G-ILC is present. Furthermore, without the G-ILC the FEC thresholds cannot be met.

The use of G-ILC pre-compensation with only conventional linear post-compensation (MMSE only,  $\times$  markers) allows 32-QAM to come under the 20% FEC threshold; it has small improvement for 16-QAM. Adding memory polynomial nonlinear post-processing ( $\circ$  markers) helps 32-QAM, and it moves the 16-QAM performance safely below the 7% FEC threshold. The addition of the low-pass filter/MLSD post-compensation stage (+ markers) provides good extra margin to both constellations. Our line rate of 1 Tb/s translates to 833 Gb/s net.

### 5. Conclusion

We experimentally reported dual polarization 16QAM and 32QAM at 100 Gbaud with a SiP IQ modulator achieving the net rate of 833 Gb/s. To the best of our knowledge, this is highest reported bit rate for all-silicon modulator.

### 6. Acknowledgements

This work was supported by Huawei Canada and NSERC (CRDPJ 486716-15). The authors thank MICRAM for providing us with a DAC10004. We also thank CMC Microsystems for enabling the chip fabrication.

### References

1. K. Schuh, et al. 'Single Carrier 1.2 Tbit/s Transmission over 300 km with PM-64 QAM at 100 Gbaud', in OFC 2017, pp. Th5B.5.
2. R. W. Going, et al., '1.00 (0.88) Tb/s per wave capable coherent multi-channel transmitter (receiver) InP-based PICs with hybrid integrated SiGe electronics', IEEE J. Quantum Electron., Art. No. 8000310, 2018.
3. S. Zhalehpour, et al., 'All-Silicon IQ Modulator for 100 GBaud 32QAM cases', OFC 2019, pp. Th4A.5.
4. H. Sepehrian, et al., 'Silicon Photonic IQ Modulators for 400 Gb/s and Beyond', J. Lightwave Technol., pp. 3078-86, 2019.
5. J. Lin, et al., 'Single-carrier 72 GBaud 32QAM and 84 GBaud 16QAM case using a SiP IQ modulator with joint digital-optical pre-compensation', Opt. Express, pp. 5610-19, 2019.
6. S. Zhalehpour, et al. 'Mitigating pattern dependent nonlinearity in SiP IQ-modulators via iterative learning control pre-distortion', Opt. Express, pp. 27639-49, 2018.
7. L. Ding, et al. 'A robust digital baseband predistorter constructed using memory polynomials', IEEE Trans. on Communications, pp. 159-165, 2004.